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Published in:
Applied Physics Letters

DOI:
[10.1063/1.3589986](https://doi.org/10.1063/1.3589986)

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Document Version
Publisher's PDF, also known as Version of record

Publication date:
2011

[Link to publication in University of Groningen/UMCG research database](#)

Citation for published version (APA):

Roelofs, W. S. C., Mathijssen, S. G. J., Raiteri, D., Geuns, T. C. T., Kemerink, M., Cantatore, E., Janssen, R. A. J., de Leeuw, D. M., & Bijleveld, J. C. (2011). Fast ambipolar integrated circuits with poly(diketopyrrolopyrrole-terthiophene). *Applied Physics Letters*, 98(20), 203301-1-203301-3. [203301]. <https://doi.org/10.1063/1.3589986>

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Fast ambipolar integrated circuits with poly(diketopyrrolopyrrole-terthiophene)

W. S. C. Roelofs,^{1,2,a)} S. G. J. Mathijssen,^{2,3} J. C. Bijleveld,¹ D. Raiteri,¹ T. C. T. Geuns,² M. Kemerink,¹ E. Cantatore,¹ R. A. J. Janssen,¹ and D. M. de Leeuw^{2,3,b)}

¹Eindhoven University of Technology, P.O. Box 513, 5600 MB Eindhoven, The Netherlands

²Philips Research Laboratories, High Tech Campus 4, 5656 AE Eindhoven, The Netherlands

³University of Groningen, Nijenborgh 4, 9747 AG Groningen, The Netherlands

(Received 8 February 2011; accepted 21 April 2011; published online 17 May 2011)

Ambipolar integrated circuits were prepared with poly(diketopyrrolopyrrole-terthiophene) as the semiconductor. The field-effect mobility of around $0.02 \text{ cm}^2/\text{V s}$ for both electrons and holes allowed for fabrication of functional integrated complementary metal-oxide semiconductor (CMOS)-like inverters and ring oscillators. The oscillation frequency was found to have a near quadratic dependence on the supply bias. The maximum oscillation frequency was determined to be 42 kHz, which makes this ring oscillator the fastest CMOS-like organic circuit reported to date.

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Copolymers with diketopyrrolopyrrole (DPP) units are emerging as attractive semiconducting materials for organic solar cells^{1–3} and transistors.^{4–8} In DPP based bulk-heterojunction solar cells power conversion efficiencies over 5% are obtained⁹ and high hole mobilities are found in field-effect transistors (FETs).^{4,6,7} For FETs even ambipolar operation is observed.^{4,5,8} Efficient injection and transport of both electrons and holes allows for the fabrication of complementary metal-oxide semiconductor (CMOS) logic based on ambipolar transistors, i.e., CMOS-like logic, which combines the robustness and good noise margin of truly complementary logic with the ease of processing of unipolar logic. CMOS-like logic has been demonstrated^{10,11} but the availability of an ambipolar semiconductor that exhibits both high and balanced electron and hole mobilities has been the main bottleneck to manufacture complementary logic that competes in performance with its unipolar counterpart. Recently, we reported that poly(DPP-terthiophene) (PDPP3T) [Fig. 1(a)] exhibits nearly balanced electron and hole mobilities.⁵ Here, we show the first integrated circuits based on DPP-copolymers. CMOS-like ring oscillators operating at frequencies up to 42 kHz are demonstrated. These are the fastest organic CMOS-like circuits reported to date and approach the speeds obtained in state-of-the-art organic CMOS¹² and organic unipolar^{13,14} circuits. This makes DPP-copolymers viable candidates to act as the semiconductor in high performance organic logic.

Integrated circuits were fabricated from FETs with patterned gates on a monitor wafer in a bottom-gate bottom-contact architecture [Fig. 1(a)]. To build the transistor gates and a first interconnect layer a phosphorous doped polycrystalline silicon layer (250 nm) was applied via chemical vapor deposition, structured by conventional photolithography, and thermally oxidized to yield the gate oxide (206 nm) with a gate capacitance of $17 \text{ nF}/\text{cm}^2$. Then vertical interconnects were defined by photolithography. Next titanium/gold was sputtered and patterned creating the source and drain electrodes and the second layer of interconnects. Finally,

PDPP3T was applied by spin coating, after which the stack was annealed at 140°C in vacuum for 24 h.

The SiO_2 gate dielectric is thermally grown on the polycrystalline gate, which is notoriously rough. The resulting rough dielectric surface could hamper charge transport. The atomic force microscopy (AFM) topography of the bare gate dielectric and gold source and drain contacts is presented in Fig. 1(b). The root-mean-square roughness of the bare SiO_2 dielectric is very large, about 9 nm. To study the impact of

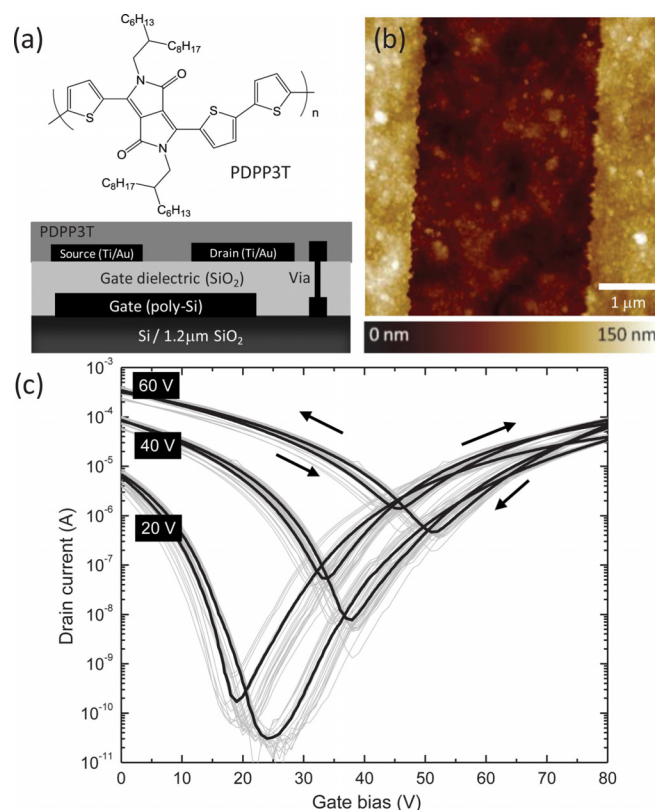


FIG. 1. (Color online) (a) Structure of PDPP3T and cross-section of the transistor and vias. (b) AFM topography of the bare SiO_2 gate dielectric on polycrystalline silicon (middle) with source and drain contacts (left and right). (c) Grey: transfer characteristics of 16 identical PDPP3T transistors ($L=5 \mu\text{m}$; $W=1000 \mu\text{m}$) measured at drain biases of 20, 40, and 60 V. Black: average of the 16 transfer characteristics.

^{a)}Electronic mail: w.s.c.roelofs@tue.nl.

^{b)}Electronic mail: dago.de.leeuw@philips.com.

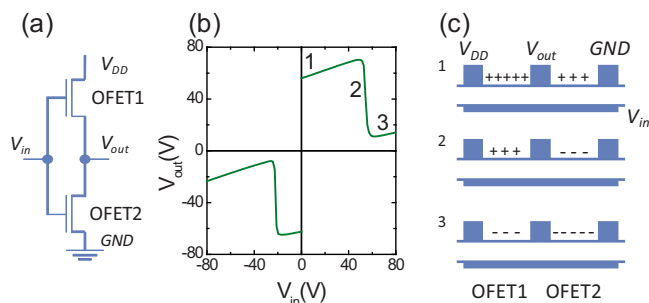


FIG. 2. (Color online) (a) CMOS-like logic inverter schematic. (b) Typical input-output characteristic of an inverter based on two identical transistors ($L=5 \mu\text{m}$, $W=100 \mu\text{m}$) measured at a supply bias V_{DD} of -80 and 80 V. (c) Schematic diagram of the operation mechanism of a CMOS-like inverter in 3 regions as indicated in (b): (1) $V_{in}=0$ V, (2) $V_{in} \approx V_{DD}/2$, and (3) $V_{in}=V_{DD}$.

this roughness on the charge transport, we fabricated 16 identical transistors, all with a channel length, L , of $5 \mu\text{m}$ and a width, W , of $1000 \mu\text{m}$. In Fig. 1(c) transfer curves of these transistors are plotted for different drain biases. The transistors exhibit similar electrical characteristics; the standard deviation in the drain current is only 10%. The averaged electron and hole mobility amounts to $0.02 \text{ cm}^2/\text{V s}$ and $0.04 \text{ cm}^2/\text{V s}$, respectively, comparable to the mobility in FETs made using atomically smooth SiO_2 .⁵ The hysteresis is slightly larger than observed before,⁵ which we tentatively ascribe to a more hydrophilic gate dielectric surface.¹⁵ The apparent insensitivity of the charge carrier mobility in PDPP3T to the gate dielectric surface roughness is remarkable in view of earlier findings where pentacene or pBTTT films were used.^{16–19} There, a mobility decrease by two orders of magnitude was reported for a similar surface roughness of 9 nm . We conjecture that the insensitivity of the charge carrier mobility in PDPP3T to the surface morphology of the dielectric is due to the amorphous nature of the film, in contrast to pentacene and pBTTT which are polycrystalline. The high mobility and uniformity of the fabricated PDPP3T transistors enables integration of multiple transistors into more complex circuits.

FETs made with PDPP3T are ambipolar, i.e., both electrons and holes can be injected using a single electrode material, here gold. The transistors allow for fabrication of integrated circuits not based on unipolar logic but on complementarylike logic instead. In CMOS-like logic an inverter is created by combining two ambipolar transistors as depicted in the Fig. 2(a). Both gates are shorted and the source of the first transistor is connected to the drain of the second. The input bias, V_{in} , is then applied to the shorted gates, while the output voltage, V_{out} , is read from the point where the source and drain of both transistors are connected. In Fig. 2(b) a typical static input/output characteristic is shown of an inverter based on two identical transistors with $L=5 \mu\text{m}$ and $W=100 \mu\text{m}$. Voltage inversion is demonstrated for both negative and positive supply biases, V_{DD} , as expected for an ambipolar inverter.

The operation mechanism of a CMOS-like inverter working in the first quadrant is schematically depicted in Fig. 2(c). An inverter is basically a voltage divider with two transistors acting as tunable resistors, controlled by the input voltage. When the input bias is low ($V_{in}=0$ V, region 1) more holes are accumulated in organic field-effect transistor 1 (OFET1) than in OFET2, making the resistance of OFET1

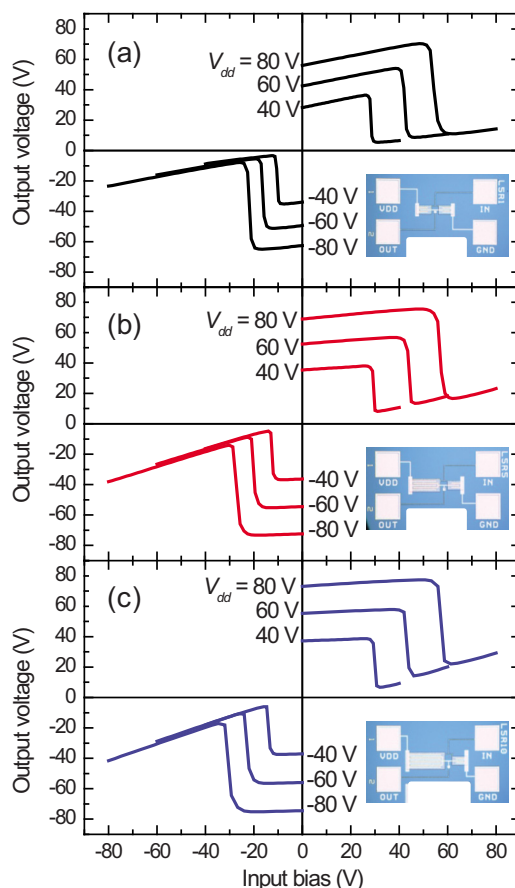


FIG. 3. (Color online) Input-output characteristics of three inverters. The width of OFET1 is increased from (a) $100 \mu\text{m}$ to (b) $500 \mu\text{m}$ and (c) $1000 \mu\text{m}$. The inset shows an optical micrograph of each inverter.

lower than that of OFET2. As a consequence, V_{out} approaches V_{DD} . When the input bias is increased to about half V_{DD} , OFET1 and 2 work in p - and n -type modes, respectively, with about equal charge density and resistivity. Hence, the output voltage is about half the input voltage. When the input bias is increased even further and approaches the supply bias ($V_{in}=V_{DD}$, region 3), more electrons are accumulated in OFET2 than in OFET1. The resistance of OFET2 is, therefore, lower than that of OFET1 and V_{out} approaches zero. The steepness of the slope of the inverter curve indicates the gain of the inverter. The present PDPP3T-based inverters have a gain around 20, which is comparable to that of state-of-the-art CMOS-like inverters and to organic inverters made on atomically smooth SiO_2 .⁵

Ambipolar transistors can never be switched off completely [Fig. 1(c)]. Due to the accumulation of charge carriers in the transistors at input voltages close to 0 V and V_{DD} , the inverter is consuming power in both states. This is a drawback of CMOS-like logic as compared to truly CMOS logic where the transistors can be switched off and the power consumption is minimal in these states. The undesirable current is reflected in a positive slope of the inverter characteristics in region 1 and 3. The slope depends on the mobility of electrons and holes and on the lateral dimensions of the two transistors. To optimize the characteristics of the inverter, we changed the geometry of the composing transistors. Figures 3(a)–3(c) shows input-output characteristics for different supply biases as the width of OFET1 in the inverter is increased from 100 to 500 , and $1000 \mu\text{m}$. When OFET1 is enlarged, a decrease of the positive slope is observed in re-

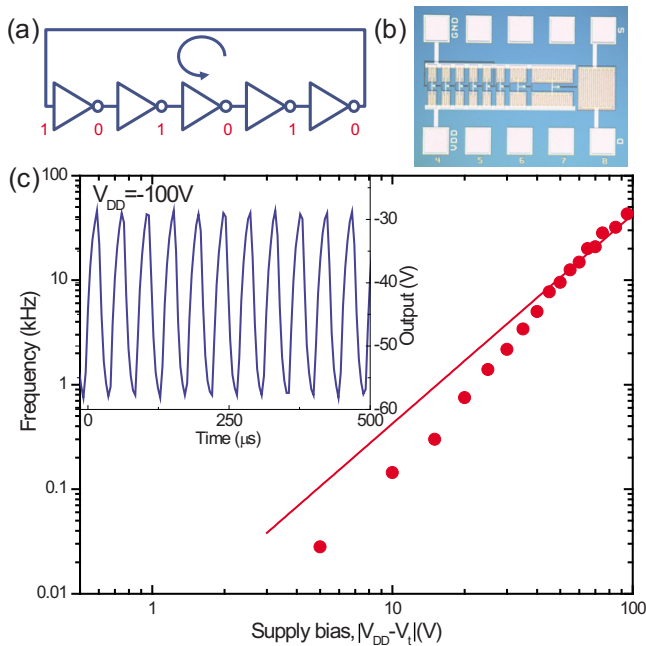


FIG. 4. (Color online) (a) CMOS-like logic ring oscillator schematic. (b) Optical micrograph of the integrated ring oscillator. (c) Log-log plot of the oscillation frequency vs supply bias (markers) with quadratic fit (line), $V_t = 35$ V. Inset: output of the ring oscillator vs. time at $V_{DD} = 100$ V, determined by measuring the current through a transistor in the buffer stage.

gion 1 while the slope in region 3 is increased. In this way the width of the transistors is a handle to optimize the inverter characteristics.

Five inverters were connected in series to create an integrated CMOS-like ring oscillator [Figs. 4(a) and 4(b)]. To read out the state of the ring oscillator a buffer stage was implemented. Three kinds of fully functional five stage ring oscillators were fabricated based on the inverters presented above. We focus on the ring oscillator comprising identical transistors, because it outperformed the other ring oscillators. The output of the oscillator as a function of time is depicted in the inset of Fig. 4(c). An oscillation frequency of about 42 kHz was obtained at a supply bias of 130 V, which makes this ring oscillator the fastest organic CMOS-like circuit reported to date.

The oscillation frequency is found to have a quadratic dependence on the supply bias for values of V_{DD} larger than about 80 V [Fig. 4(c)]. A tentative explanation follows from the waveform of the measured output voltage of the ring oscillator, V_{out} , which exhibits a saw-tooth shape [Fig. 4(c) inset]. This shape implies that the pull-up and pull-down transistors are always in saturation [like in Fig. 2(b)-region 2). The saturated current of one inverter stage is used to charge the capacitance, C_L , of the next inverter stage. Current conservation then yields²⁰

$$\frac{\mu C_{ox} W}{2L} (V_{DD} - V_t)^2 = -C_L \frac{dV_{out}}{dt}, \quad (1)$$

where V_t , μ , and C_{ox} are the threshold voltage, charge carrier mobility, and the gate oxide capacitance, respectively. The charging time or stage delay time can then be calculated by integrating Eq. (1). The oscillation frequency, f , which is proportional to the inverse of the stage delay time, is then given by

$$f \sim \frac{\mu C_{ox} W}{4L C_L \Delta V_{out}} (V_{DD} - V_t)^2 C_{ox}. \quad (2)$$

With $\Delta V_{out} = \int_{V_{min}}^{V_{max}} dV_{out}$, where V_{max} and V_{min} are the maximum and minimum output voltages during the oscillation, respectively. The effective mobility for electrons and holes was measured to be nearly constant at gate biases larger than 80 V. Hence for large biases a quadratic dependence is found in good agreement with Fig. 4(c). For smaller gate biases the mobilities are not constant but depend on the gate bias yielding a more than quadratic dependence of oscillation frequency on bias.

In summary, we demonstrated ambipolar transistors, integrated CMOS-like inverters, and ring oscillators with PDPP3T as semiconductor. The obtained oscillation frequency in ring oscillators was determined to be 42 kHz, which makes the ring oscillator the fastest organic CMOS-like circuit reported to date.

This research has received funding from NanoNextNL, from the European Community's Seventh Framework Program (FP7/2007-2013) under Grant No. 248092 of the MOMA project and is partially supported by the Dutch Technology Foundation STW.

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